HiPC 2016 Accepted Papers – By Technical Session

Preliminary Technical Program

December 19, 2016 - Day 1

HiPC 2016 Workshops

December 20, 2016 - Day 2

KEYNOTE ADDRESS:

Genomes Galore: Big Data Challenges in the Life Sciences

Srinivas Aluru, Georgia Institute of Technology, USA

Technical Session 1: Applications

Soft Error Detection for Iterative Applications Using Offline Training Jiaqi Liu and Gagan Agrawal (Ohio State University, USA)

Fault Tolerant Frequent Pattern Mining

Sameh Shohdy (The Ohio State University, USA); Abhinav Vishnu (Pacific Northwest National Laboratory, USA); Gagan Agrawal (The Ohio State University, USA)

 ${\it Parallel Performance-Energy Predictive\ Modeling\ of\ Browsers:\ Case\ Study\ of\ Servo}$

Rohit Zambre (University of California, Irvine, USA); Lars Bergstrom (Mozilla Research, USA); Laleh Aghababaie Beni and Aparna Chandramowlishwaran (University of California, Irvine, USA)

Optimization of Brain Mobile Interface Applications Using IoT

Koosha Sadeghi, Ayan Banerjee, Javad Sohankar and Sandeep K.S. Gupta (Arizona State University, USA)

Mizan-RMA: Accelerating Mizan Graph Processing Framework with MPI RMA

Mingzhe Li, Xiaoyi Lu, Khaled Hamidouche, Jie Zhang and Dhabaleswar K. (DK) Panda (The Ohio State University, USA)

CUDA M3: Designing Efficient CUDA Managed Memory-aware MPI by Exploiting GDR and IPC Khaled Hamidouche, Ammar Ahmad Awan, Akshay Venkatesh, and Dhabaleswar K. (DK) Panda (The Ohio State University, USA)

Technical Session 2: Algorithms for data and data management

Parallel Implementation of Lossy Data Compression for Temporal Data Sets

Zheng Yuan (Northwestern University, USA); William Hendrix (University of South Florida, USA); Seung Woo Son (University of Massachusetts Lowell, USA); Christoph Federrath (Australian National University, Australia); Ankit Agrawal, Wei-keng Liao and Alok Choudhary (Northwestern University, USA)

Scalable Parallel Algorithms for Shared Nearest Neighbor Clustering

Sonal Kumari, Saurabh Maurya, Poonam Goyal, Sundar S. Balasubramaniam, and Navneet Goyal (BITS-Pilani, India)

DCRoute: Speeding up Inter-Datacenter Traffic Allocation while Guaranteeing Deadlines

Mohammad Noormohammadpour and Cauligi Raghavendra (University of Southern California, USA); Sriram Rao (Microsoft, USA)

Efficient Data Redistribution to Speedup Big Data Analytics in Large Systems

Long Cheng (Eindhoven University of Technology, The Netherlands); Tao Li (TU Dresden, Germany)

Load Balancing for Molecular Dynamics Simulations on Heterogeneous Architectures

Steffen Seckler, Nikola Tchipev, Hans-Joachim Bungartz and Philipp Neumann (Technical University of Munich, Germany)

Technical Session 3: Memory and I/O

MEC: The Memory Elasticity Controller

Roberto Sawamura, Cristina Boeres and Vinod E.F. Rebello (Universidade Federal Fluminense, Brazil)

Phoenix: Memory Speed HPC I/O with NVM

Pradeep Fernando, Sudarsun Kannan, Ada Gavrilovska and Karsten Schwan (Georgia Institute of Technology, USA)

Dynamic Data Layout Optimization for High Performance Parallel I/O

Everett Neil Rush, Bryan Harris and Nihat Altiparmak (University of Louisville, USA); Ali Saman Tosun (University of Texas at San Antonio, USA)

Read Consistency in Distributed Database Based on DMVCC

Jie Shao (Tsinghua University and Baidu, Inc., P.R. China); Boxue Yin, Bujiao Chen, Guangshu Wang, Lin Yang, Jianliang Yan and Jianying Wang (Baidu, Inc., P.R. China); Weidong Liu (Tsinghua University, P.R. China)

Data Elevator: Low-contention Data Movement in Hierarchical Storage System

Bin Dong, Suren Byna, Kesheng Wu, Prabhat, Hans Johansen, Jeffrey N. Johnson, and Noel Keen (Lawrence Berkeley National Laboratory, USA)

Telescoping Architectures: Evaluating Next-Generation Heterogeneous Computing Konstantinos Krommydas and Wu-chun Feng (Virginia Tech, USA)

December 21, 2016 – Day 3

KEYNOTE ADDRESS:

China's HPC development in the next 5 years

Depei Qian, Sun Yat-sen University and Beihang University, China

Technical Session 4: Numerical applications

CMT-bone - A Proxy Application for Compressible Multiphase Turbulent Flows

Tania Banerjee, Jason Hackl and Mrugesh Shringarpure (University of Florida, USA); Tanzima Islam (Lawrence Livermore National Laboratory, USA); S. Balachandar, Thomas Jackson and Sanjay Ranka (University of Florida, USA)

Balancing locality and concurrency: solving sparse triangular systems on GPUs $\,$

Andrea Picciau, Gordon E. Inggs, John Wickerson, Eric C. Kerrigan and George Constantinides (Imperial College UK, United Kingdom)

Tensor Contractions with Extended BLAS Kernels on CPU and GPU

Yang Shi, U.N. Niranjan and Animashree Anandkumar (University of California, Irvine, USA); Cris Cecka (NVIDIA Research, USA)

High performance Horizontal Diffusion Calculations in Ocean Models on Intel® Xeon Phi™ Coprocessor Systems Aketh TM, Sathish Vadhiyar, PN Vinayachandran, and Ravi Nanjundiah (Indian Institute of Science, Bangalore, India)

Memory-Efficient Parallel Simulation of Electron Beam Dynamics Using GPUs

Kamesh Arumugam, Alexander Godunov, Desh Ranjan, Balsa Terzić and Mohammad Zubair (Old Dominion University, USA)

Cache-friendly Design for Complex Spatially-variable Coefficient Stencils on Many-core Architectures Jiarui Fang, Haohuan Fu and Guangwen Yang (Tsinghua University, P.R. China)

Technical Session 5: Resilience and compilers

Using Message Logs and Resource Use Data for Cluster Failure Diagnosis

Edward Chuah (The Alan Turing Institute and University of Warwick, U.K., and Singapore Polytechnic, Singapore); Arshad Jhumka (University of Warwick, United Kingdom); James C. Browne (UT Austin, USA); Nentawe Gurumdimma (University of Jos, Nigeria and University of Warwick, United Kingdom); Sai Narasimhamurthy (Seagate Technology, United Kingdom); Bill Barth (The University of Texas at Austin, USA)

A Low-Cost Multi-Failure Resilient Replication Scheme for High Data Availability in Cloud Storage Jinwei Liu and Haiying Shen (Clemson University, USA)

PRESAGE: Protecting Structured Address Generation against Soft Errors

Vishal Sharma and Ganesh Gopalakrishnan (University of Utah, USA); Sriram Krishnamoorthy (Pacific Northwest National Laboratory, USA)

MP-Index: A Multi-Predicate Publish/Subscribe Mechanism for Internet of Things

Satvik Patel (Parul University, India); Sunil Jardosh (Progress Software, India); Ashwin Makwana (CHARUSAT University, India)

Phase Directed Compiler Optimizations

Era Jain (IIT Kanpur (Now at Google), USA); Subhajit Roy (Indian Institute of Technology, Kanpur, India)

Automatic Code Generation for Iterative Multi-dimensional Stencil Computations

Mariem Saied and Jens Gustedt (INRIA and ICube Université de Strasbourg, France); Gilles Muller (INRIA and LIP6 – Sorbonne Universités, CNRS, UPMC, France)

December 22, 2016 - Day 4

KEYNOTE ADDRESS:

Toward Extreme-Scale Processor Chips

Josep Torrellas, University of Illinois Urbana-Champaign, USA

Technical Session 6: Parallel algorithms: Data structures, resource allocation, and linear algebra

Fast Parallel Operations on Search Trees

Yaroslav Akhremtsev and Peter Sanders (Karlsruhe Institute of Technology, Germany)

Efficient Parallel Ear Decomposition of Graphs with Application to Betweenness-Centrality

Charudatt Pachorkar, Meher Chaitanya, and Kishore Kothapalli (International Institute of Information Technology, Hyderabad, India); Debajyoti Bera (Indraprastha Institute of Information Technology, Delhi, India)

Parallelization of Bin Packing on Multicore Systems

Sayan Ghosh and Assefaw H. Gebremedhin (Washington State University, USA)

Scheduling of Linear Algebra Kernels on Multiple Heterogeneous Resources

Olivier Beaumont, Terry Cojean, Lionel Eyraud-Dubois, Abdou Guermouche, and Suraj Kumar (INRIA Bordeaux Sud-Ouest and University of Bordeaux, France)

An Alternative Approach of the SPIKE Preconditioner for Finite Element Analysis

Leonardo Muniz de Lima, and Brenno Albino Lugon and Lucia Catabriga (Universidade Federal do Espírito Santo, Brazil)

Technical Session 7: Software architecture

Compiler Support for Software Cache Coherence

Sanket Tavarageri (The Ohio State University, USA); Wooil Kim and Josep Torrellas (University of Illinois at Urbana-Champaign, USA); P Sadayappan (The Ohio State University, USA)

Predictive Evaluation of Partitioning Algorithms Through Runtime Modelling Richard A. Bunt, Stephen A. Wright and Stephen A. Jarvis (University of Warwick, United Kingdom); Yoon K. Ho and Matthew J. Street (Rolls-Royce, United Kingdom)

Performance Prediction of Parallel Applications Based on Small-Scale Executions Rodrigo Escobar and Rajendra V. Boppana (University of Texas at San Antonio, USA)

ERICO: Effective Removal of Inline Caching Overhead in Dynamic Typed Languages Gem Dot (Universitat Politècnica de Catalunya, Spain); Alejandro Martínez (ARM, United Kingdom); Antonio González (Universitat Politècnica de Catalunya, Spain)

A Directory Cache with Dynamic Private-Shared Partitioning
Joan Valls and María Engracia Gómez (Universidad Politecnica de Valencia, Spain); Alberto Ros (University of Murcia, Spain); Julio Sahuquillo (Universidad Politecnica de Valencia, Spain)

Steal-A-GC: Framework to Trigger GC during Idle Periods in Distributed Systems Sujoy Saraswati, Soumitra Chatterjee and Ranganath Ramachandra (HPE, India)