

## HiPC 2016 Student Parallel Programming Challenge Intel Track

#### **Training Material and Sessions**

To help with getting the best performance on Intel architectures we present a three part Video set and resources that help you to :

- 1. Part 1 : Introduction to Parallel Programming
- 2. Part 2 : Intel Software tools and programming methodology for Intel® Xeon Phi™
- 3. Part 3 : The 2<sup>nd</sup> Generation Intel<sup>®</sup> Xeon Phi<sup>™</sup> (Knights Landing) architecture and programming

Intel will also host a web-chat "Meet the HPC experts session" on the 17<sup>th</sup> of October 2016 from 2PM – 4PM to help participants with clarifications and queries they might have on various aspects related to improving performance on their codes. Here is the link for registering for the session:

https://attendee.gotowebinar.com/register/2240951310200227843

#### Intel tools

Intel® Parallel Studio XE 2016 is a software development suite that helps boost application performance by taking advantage of the ever-increasing processor core count and vector register width available in Intel® Xeon® processors, Intel® Xeon Phi<sup>™</sup> coprocessors and compatible processors.

To download 30 day full featured evaluation of the tools to optimize your code visit:

https://software.intel.com/en-us/intel-parallel-studio-xe/try-buy

#### **Training Videos**

#### Part-1 of Training: Introduction to Parallel Programming

Sl.no	Topics
1.	Why Parallel? Why Now?
2.	Finding Parallelism
3.	Shared Memory Considerations
4.	Confronting Race Conditions

5.	<u>Deadlocks</u>
6.	OpenMP for Task Decomposition
7.	Reducing Parallel Overhead

### Part-2 of Training: Intel Software tools and programming methodology for Intel<sup>®</sup> Xeon Phi<sup>™</sup>

Sl.no	Topics
1.	Programming for Today and Tomorrow, Not Yesterday
2.	<u>Create Faster Code Faster – Intel® Parallel Studio XE 2017</u>
3.	Vectorization Advisor
4.	Optimize for AVX-512 with or without AVX-512 hardware
5.	Advanced Topics in Vector Programming
6.	Intel® Threading Building Blocks (Intel® TBB)
7.	Best Practices in Vector Programming
8.	<u>3 Keys to HPC Performance</u>
9.	Additional Videos Published by Colfax International on Intel® Xeon Phi <sup>TM</sup> Coprocessors.

# Part-3 of Training: The 2<sup>nd</sup> Generation Intel<sup>®</sup> Xeon Phi<sup>™</sup> (Knights Landing) architecture and programming

Sl.no	Topics
1.	Knights Landing: The Second Generation Intel® Xeon Phi <sup>TM</sup>
2.	An Intro to MCDRAM (High Bandwidth Memory) on Knights Landing
3.	<u>Knights Landing – An Overview for Developers</u>