हाइपीसी HiPC

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Intel @ HiPC 2013

Venue: **Park Plaza, Bangalore**

Date: **20th December 2013**

About HiPC 2013

The 20th IEEE International Conference on High Performance Computing (HiPC 2013) provides an ideal platform for presenting current work by researchers from around the world as well as to highlight activities in Asia in the area of high performance computing.

Intel's 'Birds of a Feather' Sessions

1 Session

Performance productivity challenges and researches for the future of computing - By Victor Lee

Abstract: Over the past few decades, compute performance has been improving steadily due to the advancements in semiconductor manufacturing technology, circuit design and computer architecture. We expect the technology treadmill to continue providing us with innovations that would take us to Exascale computing within this decade. Many technology advances that brought us the performance improvement have also increased the level of complexity programmers must deal with. Similar trends in other technology areas will make performance productivity one of the grand challenges in the future of computing. This talk will discuss technology trends for future computing and how these trends have created performance productivity challenges for developers. It will also provide a survey of researches that academia and industry have started to overcome these challenges.

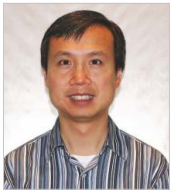
2 Session

Xeon-Phi Performance for Real World Applications – By Dr. Paresh Pattani

Abstract: This talk will discuss applications performance on Intel® Xeon Phi™ for Numerical Weather Simulation, Life Sciences, Oil & Gas, Manufacturing and Financial Services verticals. Performance of key applications, programming models and parallelization/ vectorization methodology will also be presented.

About the Speakers

Victor Lee



Victor Lee received a B.S. in Electrical Engineering from University of Washington in 1994, an S.M. in Electrical Engineering and Computer Science from Massachusetts Institute of Technology in 1996. He joined Intel Corporation in 1997 where he worked on the Intel® Pentium® Pro, the Intel® Pentium® 4 Processor, the Intel® Itanium® Processor and the QPI Interconnect Architecture. He is also a key contributor to the Intel Many Integrated Core Architecture and a member of the Intel® Xeon Phi™ Coprocessor design team. Victor is an IEEE senior member, a principal engineer and research scientist in Intel's Parallel Computing Lab. His research interests include computer architecture, parallel algorithms and applications and auto-tuning.

Dr. Paresh Pattani

Dr. Paresh Pattani is Director, Data Center Computing, in Intel Corporation's Software & Services Group (SSG). Paresh has been with Intel for 13 years in Software & Services Group. Paresh has 20+ years industry experience in Data Center space and manages engineering teams enabling Enterprise, Big Data, Cloud and HPC verticals such as Manufacturing, Energy, Financial Services, Life Sciences and Digital Content Creation segments. He is leading the customer enabling for Intel® Xeon®, Intel® Xeon Phi™ and Microserver platforms.

Paresh has a Ph.D. in Civil Engineering with specialization in computational mechanics from the University of British Columbia, Vancouver, Canada. He has an MBA from University of Texas at Austin and Bachelor of Technology from Indian Institute of Technology, Mumbai, India.

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