HiPC-2003: Industrial Keynote Talks

Thursday, Dec. 18th 2003, 5pm-7pm

Real-Time Collaboration: The Next Wave on the IP Networks

Ramu V. Sunkara, Vice President, Oracle Corporation

Abstract: What is the world's most sophisticated computing system? The Internet. It comprises of several IP Networks with all kinds of computers on this system. Every corporation, educational institution, and government has an IP network of itself. Now, with the advent of wireless networks, every cell phone, PDA, Laptop and TV will be part of this ever-growing computing system. What is the next wave of technology to build on the ever-present, ubiquitous IP networks?

Oracle believes that Real-Time Collaboration will be the next big wave for the Internet. Early versions of VoIP, IM, SMS, and Web Conferencing have proved to be very valuable to all classes of users in all societies. The next generation of these software products poses a very difficult technical challenge: how do you get data, voice, and video in real-time (milliseconds), over these IP networks, on the worlds most sophisticated computer system, the Internet? How do you do this in a reliable 24X7 manner like the telephone system ?

In this talk, we will outline Oracle's vision of the future of this technology and market space, and its immediate plans to set up an R&D arm in India. The talk will feature a live demo: it will be broadcast in real-time on the worldwide web using Oracle Web Conferencing.

Ramu V. Sunkara is Vice President at Oracle in charge of the Real-Time Collaboration Products division. Ramu started this division in 2001 seeing the market opportunity for Oracle and the evolution of the Internet & Intranets. Prior to this, Ramu was the Vice President for Technology and Architecture at Oracle e-Business Suite CRM products. During his 18-month tenure, he evolved the Oracle e-Business Suite HTML & Java Technology stack by delivering 4 versions of the software. Earlier Ramu led software development and Product Management for Oracle Portal Engine, Oracle iCache, Oracle Fail Safe, and Oracle Parallel Server products. Before joining Oracle in 1995, Ramu pioneered the development of several Relational Database products at Digital Equipment Corporation. He has over 16 patents granted by the US PTO in the areas of Caching for Internet Services, Parallel Databases, Fault-Tolerant Systems, Query Processing, etc. Ramu has a B.Tech. degree from IIT-Madras, an MS (Computer Science) from UW-Madison and an MBA from Boston University.

High Performance Computing and Windows

Amit Chatterjee, Director, Windows Group
Microsoft India Development Center

Abstract: This talk covers where HPC is today, what's driving the changes, and what the Windows platform & its partners have to offer for HPC in terms of platform, value, and performance.

Amit Chatterjee is the Director of the Windows Group in Microsoft's India Development Center in Hyderabad. He owns the product vision and delivery of several important Windows server and client technologies like Services for UNIX, Windows System Resource Manager, Routing and Remote Access Service, and Fax.

Amit joined Microsoft in 1988, and has worked on and led several strategic products for the Company. Starting his career at Microsoft as part of the Windows 2.1 development team, Amit spent several years being a key member of the Windows team that shipped Windows 2.1, 3.0, 3.1, and Windows 95. Amit was the development manager for GDI and printing teams for Windows 95, Direct Show and DirectX Media technologies, and holds several patents in the Graphics area.

After 11 years in Redmond, Amit joined the India Dev. center and has been an integral part of it since its inception. Amit was instrumental in starting and delivering several of the projects that the center owns today. Amit holds a B. Tech in E&ECE and M. Tech in Computer Eng. from Indian Institute of Technology Kharagpur.

High Performance Microprocessors – The Design Challenge

Sunil Kakkar, IBM Global Services

Abstract: Processor Architecture has evolved in a big way from the days of the simple RISC machine. Today's processors are capable of fetching multiple instructions at the same time, each instruction comprising of multiple operations and executing these operations in parallel very efficiently.

Most of the modern processors today have a complex pipeline architecture for higher performance needs, the complexity arising from several functional units operating simultaneously inside the processor which can fetch many instructions at the same time and then speculatively execute them in these functional units, not necessarily in order.

The verification effort grows exponentially as the design complexity grows linearly. Due to verification issues, the design costs are spinning out of control, especially for high performance processors. It is commonplace today for a processor design to have 100 million gates at 90 nm but consider the fact that a one million gate design requires 5 - 8 verification engineers. Server farms of thousands of PCs are needed to run simulation tests around the clock. A mask costs at least $600,000 at 130 nm and double that at 90 nm and hence you cannot afford to have a silicon respin. It is a thing of the past that 50% of the effort on a chip design is spent on verification. Today the percentage is more like 80% and is likely to skyrocket in the near future.
All this opens up new frontiers of challenges in verifying the complex processor architectures of today with all the practical constraints that are placed on the verification team. We will talk about what is available to ease this burden (including modern Formal Verification techniques) and what steps a verification engineer may take to ensure a bug-free, reliable design.

Sunil Kakkar currently heads the High Performance Hardware Verification Group at IBM Global Services in Bangalore and is the lead technologist for the IBM's e-verification technology initiative in the Asia-Pacific region. He has over 20 years of experience in Processor Design, Architecture, Performance and Functional Verification. Prior to IBM, Sunil has worked for companies like Hewlett Packard, IDT and Sony and was a key verification architect at Transmeta for the Efficeon Processor. Sunil has taught at the UC Berkeley program for industry professionals, and was invited to chair the IEEE Computer Society Conference session on Verification.
Sunil holds a Bachelor's degree from IIT-Kanpur and two Master's degrees from the University Of Illinois.