Workshop on Cutting Edge Computing

Advance Programme

December 17, 2003 (Wednesday), 9:30 am to 1:00 pm
at Hotel Taj Krishna, Hyderabad, India.

Cochairs:

Uday S. Shukla
IBM Software Labs, India.
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Rajendra K. Bera
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INVITED TALKS

9:30 am – 10:30 am
Arun K. Pati (Institute of Physics, Bhubaneswar, India)
Quantum mechanical personal computers

ABSTRACT

Quantum computers exploit the linear superposition principle which allows us to carry out massive computations in parallel and quantum entanglement possibly gives the desired speed-up compared to their classical counterparts. However, the linearity of the evolution of quantum states imposes fundamental limitations on possible operations that one can perform on a quantum bit or qubit—the basic unit of quantum information. Unlike a classical bit, a qubit cannot be copied perfectly. Interestingly, we cannot even record a qubit, whereas classically we can keep a record of a bit. Furthermore, given two identical qubits one cannot delete a copy against the other, whereas classically one can always delete a copy from two copies of a bit in a reversible manner. In addition, we can perform a NOT operation on a classical bit perfectly, whereas on a qubit we cannot implement a NOT operation. Also, we will argue that it is impossible to design a XOR gate for two unknown qubits. Further, we will prove that one cannot design universal Hadamard gate for creating equal superposition of the original and its complement state. Considering all these limitations it appears that ultimate quantum computers will be inherently personal. This gives rise to a notion of quantum mechanical personal computers (QPCs) that are fundamentally different from classical PCs. The security of personal information stored in a quantum computer which is a single user QPC comes from fundamental principles of quantum theory rather than my man-made design.

10.30 am - 11.00 am
Coffee/Tea Break.

11:00 am – 12:00 noon
Uday Khedker (Indian Institute of Technology, Bombay, India) and
R. Govindrajan (Indian Institute of Science, Bangalore, India)

Compiler analysis and optimizations: What is new?

ABSTRACT

Traditional compiler analyses and back-end optimizations, which play an important role in generating efficient code for modern high-performance processors, are quite mature, well understood, and have been widely used in production compilers. However, recent advances in high-performance (general purpose) processor architecture, emergence of novel architectural paradigms, emphasis on application-specific processors and embedded systems, and the increasing trend on compiling applications directly onto silicon present several interesting challenges and opportunities in high performance compilation techniques. In this paper we discuss the trends that are emerging to meet the above challenges. In particular, we discuss recent advances in data flow analyses, compiling techniques for embedded and DSP processors, and compiling techniques that reduce power consumption.

12:00 noon – 01:00 pm
Nagesh R. Iyer, J. Rajasankar, and G. S. Palani (Structural Engineering Research Centre, Chennai, India)
Finite Element Modelling for Structural Dynamics Problems

ABSTRACT

The objectives of an analysis have to be defined well before the decision is made about the type of analysis to be performed. This is more critical for dynamic analyses than for static analyses. An unnecessarily fine mesh will be unduly costly. On the other hand, the model must provide the necessary and reliable results. These questions become more significant for dynamic analysis because then the costs can be significantly greater. Dramatic advances in engineering practice can be expected only if these powerful tools are put to proper use. Some fundamental aspects of modelling for dynamic analysis using the Finite Element Method are addressed, in particular those that are related to engineering practice, in this paper. The core of the entire dynamic analysis is how to produce the best and optimal finite element mesh that will yield acceptable solutions. In order to remove the uncertainty and bring in scientific and mathematical basis, *a posteriori* error estimation with adaptive mesh refinement techniques have been proposed in the paper that produce reliable finite element solutions with user acceptable accuracy.

01.00 pm – 02.00 pm
Lunch.

ABOUT THE SPEAKERS

Arun K. Pati

Please visit: http://www.informatics.bangor.ac.uk/~akpati/

Uday Khedker

Uday Khedker received his Bachelor of Engineering in Electronics & Telecom. Engg. from Jabalpur University in 1986, Master of Technology in Computer Science from Pune University in 1989 and Ph.D. in Computer Science & Engg. from IIT Bombay in 1995. He taught at the Department of Computer Science at Pune University from 1984 to 2001. Since 2001 he is with IIT Bombay where he is presently an associate professor of Computer Science & Engg. His areas of interest are programming languages and compilers and he specialises in data flow analysis and

its applications to code optimization. He has also worked very closely with the industry and is the chief architect of an optimizing compiler for Intel's IXS1000 Media Signal Processor.

R. Govindrajan

R. Govindarajan is an associate professor in the Supercomputer Education and Research Centre and in the Department of Computer Science and Automation, Indian Institute of Science. He received his B.Sc. degree from Madras University in 1981, his B.E. (Electronics and Communication) and his Ph.D. (Computer Science) degrees from the Indian Institute of Science in 1984 and 1989, respectively. He was a post-doctoral research fellow at the University of Western Ontario, London, Ontario, Canada from 1989-90 and at McGill University, Montreal, Quebec, Canada from 1990-92. He worked as an assistant professor at McGill University from 1992-94 and at Memorial University of Newfoundland, St. John's, NF, Canada from 1994-95. His current research and teaching interests are in the areas of computer architecture, distributed shared memory architectures, cluster computing, compilation techniques for instruction-level parallelism, and compilation techniques for DSP and embedded processors. He is a Senior Member of IEEE and a Member of ACM SIGARCH.

Nagesh R. Iyer

Nagesh Iyer received his masters and doctoral degrees from the Indian Institute of Science, Bangalore. He is currently the deputy director and head of computational structural dynamics group and networking facility. He has over 25 years of experience in the analysis and design of large complex structures. He received the CSIR Technology Prize 1999 in engineering technology for his contribution in the development of advanced computational methodologies, modelling techniques and software for analysis and design of complex structures. He is also a recipient of the Institution of Engineers (India) aerospace engineering division’s gold medal for his paper “Analysis of ship-water interaction effect”. He is a fellow of the Institution of Engineers (India) and is listed in the Directory of Distinguished Computer Professionals of India.

J. Rajasankar

Not received.

G. S. Palani

G. S. Palani received his bachelor’s and master’s degrees in civil engineering and structural engineering, respectively, from PSG College of Technology, Coimbatore. Since the past 15 years he has been working as a scientist at the Structural Engineering Research Centre, Chennai. His fields of specialization include development of advanced finite element analysis techniques, fatigue and fracture analysis and dynamic analysis of structures. He has published about 30 papers.