HiPC 2003 Advance Program

Days at a Glance

Wednesday Dec. 17

- **Workshops**
- **Tutorials**

Thursday Dec. 18 - Program

- **8:30 a m - 9:00 a m**
  Inauguration and Opening Remarks
- **9:00 a m - 10:00 a m**
  Keynote Address
  "Life's Duplicities: Sex, Death & Valis"
  Speaker: Bud Mishra, New York University
- **10:30 a m - 12:30 p m**
  Parallel Technical Sessions I & II
- **1:30 p m - 2:30 p m**
  Keynote Address
  "The High Performance Microprocessor in the Year 2013: What will it look like? What it won't look like?"
  Speaker: Yale Patt, University of Texas at Austin
- **2:45 p m - 4:45 p m**
  Parallel Technical Sessions III & IV
- **5:00 p m - 7:00 p m**
  "Real-time Collaboration: The Next Wave on the IP Networks"
  Speaker: Ramu Sankara, Oracle Corporation

  "High Performance Computing and Windows"
  Speaker: Amit Chatterjee, Microsoft Corporation

  "High Performance Microprocessors - The Design Challenge"
  Speaker: Sunil Kakkar, IBM Global Services

Friday Dec. 19 - Program

- **8:30 a m - 9:30 a m**
  Keynote Address
  "Energy Aware Algorithm Design via Probabilistic Computing: From Algorithms and Models to Moore's Law and Novel (Semiconductor) Devices"
  Speaker: Krishna V. Palem, Georgia Institute of Technology
- **10:00 a m - n o o n**
  Parallel Technical Sessions V & VI
- **1:00 p m - 2:00 p m**
  Keynote Address
  "High Performance Computing Challenges in the Environmental Sciences"
  Speaker: Per Nyberg, Cray Inc.
- **2:00 p m - 2:30 p m**
  Poster Set-up
- **2:30 p m - 5:00 p m**
  Poster/Presentation Session
- **6:30 p m - 9:30 p m**
  Conference Banquet

Saturday Dec. 20 - Program

- **8 :3 0 a m - 9 :3 0 a m**
  Keynote Address
  "Standards Based High Performance Computing"
  Speaker:David Scott, Intel Corporation
- **1 0 :0 0 a m - n o o n**
  Parallel Technical Sessions VII & VIII
- **1 :0 0 p m - 2 :0 0 p m**
  Keynote Address
  "One Chip, One Server: How do we Exploit its Power?"
  Speaker: Per Stenstrom, Chalmers University of Technology, Sweden
- **2 :3 0 p m - 4 :3 0 p m**
  Parallel Technical Sessions IX & X

Contributed Papers
There will be 48 contributed papers from 11 countries, chosen from 164 papers submitted in response to the call for papers. Contributed papers will be presented in 10 sessions.

Exhibits
Exhibits will be open from 10:00 am to 6:00 pm on Dec. 18 and 19.

Wednesday Dec. 17

WORKSHOPS

9:00 a m - 1:00 p m

Workshop I

Workshop on Bioinformatics and Computational Biology

Discovery of biomolecular sequences and their relation to the functioning of organisms have created a number of challenging problems for computer scientists, and led to the emerging interdisciplinary field of bioinformatics and computational biology. The field holds immense potential for aiding in future discoveries such as the design of proteins for efficient administering of drugs and personalized medicine. The goal of this workshop is to provide a forum for researchers and practitioners to discuss recent research and developments in bioinformatics and computational biology. The workshop will include contributed papers and invited talks. Papers reporting on original research (both theoretical and experimental) in all areas of bioinformatics and computational biology are sought. Surveys of important recent results and directions are also welcome.

9:00 a m - 1:00 p m

Workshop II

Workshop on Cutting Edge Computing

The half-day workshop will feature invited presentations from experts in such areas as Quantum Computing, Supercomputing/Autonomic Computing, Datamining of Scientific Data, etc. The goal is to bring to the attention of researchers and practitioners, recent R&D advances in computing technologies that are expected to dominate the future of computing.

9:00 a m - 1:00 p m

Workshop III

Workshop on Soft Computing

The Workshop on Soft Computing is the second in the series and is a step towards sharing the research results and new directions in the application and convergence of the areas of Fuzzy Logic, Neural Networks, Evolutionary Computing, Probabilistic computing, Chaotic Computing and Machine Learning. In this workshop which is held along with the HiPC 2003, we intend to provide a platform for Soft Computing researchers for discussion and presentation of their work.

9:00 a m - 1:00 p m

Workshop IV

Trusted Internet Workshop

In recent years, there has been a tremendous push from both civil and military communities for next generation applications demanding Quality of Service (QoS), reliability, and security guarantees. The goal of Trusted Internet workshop is to provide a forum for researchers and practitioners to present and discuss their work and exchange ideas in the areas of Internet QoS, Internet Reliability, and Internet Security.

2:00 p m - 6:00 p m

Workshop V

Workshop on Autonomic Applications

The objective of the Autonomic Applications Workshop is to establish a forum to investigate the research issues and enabling technologies toward the convergence of biological, technological and information systems (called Autonomic Computing). Autonomic computing research will enable the design of the next generation of applications that are capable of managing, controlling and optimizing themselves. This workshop will focus on the research issues and challenges facing the development of autonomic applications that are self-defining, self-configuring, self-healing, self-optimizing, self-anticipating, contextually aware of their environments, and open.

2 :0 0 p m - 6 :0 0 p m
Workshop VI
Workshop on e-science (Grid Computing and Science Applications)
The objective of the e-science Workshop is to address the issues related to development of e-science infrastructure, Grid Middleware , Scientific Application and other related issues.

2 :0 0 p m - 6 :0 0 p m
Workshop VII
Workshop on Embedded Systems for Media Processing
Multimedia systems represent a significant part of real-time embedded systems research. Because of the the data sizes, parallelism, signal processing aspects, and soft real-time constraints, multimedia systems are a distinguishable subset of embedded systems. The goal of the workshop is to explore hardware/software/architecture issues and applications of multimedia embedded systems.

WORKSHOPS CHAIR

C.P. Ravikumar, Texas Instruments India,
Internet: **ravikumar@india.ti.com**

TUTORIALS

- **9 :0 0 a m - 1 :0 0 p m**
  Tutorial I
  System Support for Sensor based Applications

- **9 :0 0 a m - 1 :0 0 p m**
  Tutorial II
  Multimedia System Design: Providing Quality Services

- **9 :0 0 a m - 1 :0 0 p m**
  Tutorial III
  Very High Performance Cache based Techniques for Iterative Methods

- **2 :0 0 p m - 6 :0 0 p m**
  Tutorial IV
  Storage Architectures

- **2 :0 0 p m - 6 :0 0 p m**
  Tutorial V
  Mobile Ad Hoc and Sensor Networks

- **2 :0 0 p m - 6 :0 0 p m**
  Tutorial VI
  Information Security

TUTORIALS CHAIR

Srinivas Aluru, Iowa State University.
Internet: **aluru@iastate.edu**

Thursday Dec. 18

8:30 a.m - 9:00 a.m
INAUGURATION

Opening Remarks
Viktor K. Prasanna
M. Vidyasagar
Timothy Pinkston

Guest of Honor
Rajeev Sangal
Director, International Institute of Information Technology, Hyderabad

9:00 a.m - 10:00 a.m
KEYNOTE ADDRESS
"Life's Duplicities: Sex, Death & Valis"
Bud Mishra
New York University

10:30 a.m - 12:30 p.m
SESSION I
Performance Issues and Power-Aware Architectures
Chair : **Rajeev Kumar**
Indian Institute of Technology, Kharagpur

Performance Analysis of Blue Gene/L using Parallel Discrete Event Simulation
Ed Upchurch, Paul L. Springer, Maciej Brodowicz, and T. D. Gottschalk, California Institute of Technology, USA

An Efficient Web Cache Replacement Policy
A. Radhika Sarma and R. Govindarajan, Indian Institute of Science, India

Timing Issues of Operating Mode Switch in High Performance Reconfigurable Architectures
Rama Sangireddy, Huesung Kim, and Arun K. Somani, Iowa State University, USA

Power-Aware Adaptive Issue Queue and Register File
Jaume Abella and Antonio Gonzalez, Universitat Politecnica de Catalunya, Spain

FV-MSB: A Scheme for Reducing Transition Activity on Data Buses
Dinesh C. Suresh, Jun Yang, Chuanjun Zhang, Banit Agrawal, Walid Najjar, University of California, Riverside, USA

10:30 a.m - 12:30 p.m
SESSION II
Parallel/Distributed and Network Algorithms
Chair: **Javed I. Khan**
Kent State University

A Parallel Iterative Improvement Stable Matching Algorithm
Enyue Lu and S. Q. Zheng, University of Texas at Dallas, USA

Self-Stabilizing Distributed Algorithm for Strong Matching in a System Graph
Wayne Goddard, Stephen T. Hedetniemi, David P. Jacobs, and Pradip K. Srimani, Clemson University, USA

Parallel Data Cube Construction: Algorithms, Theoretical Analysis and Experimental Evaluation
Ruoming Jin, Ge Yang, and Gagan Agrawal, Ohio State University, USA

Efficient Algorithm for Embedding Hypergraphs in a Cycle
Qian-Ping Gu and Yong Wang, Simon Fraser University, Canada

Mapping Hypercube Computations onto Partitioned Optical Passive Star Networks
Alessandro Mei, Universita di Roma "La Sapienza", Italy, Romeo Rizzi, University of Trento, Italy

1:30 pm - 2:30 pm
KEYNOTE ADDRESS
"The High Performance Microprocessor in the Year 2013: What will it look like? What it won't look like?"
Yale Patt
University of Texas at Austin

2:45 pm - 4:45 pm
SESSION III
Routing in Wireless, Mobile, and Cut-Through Networks
Chair: **Pradip K Srimani**
Clemson University

FROOTS - Fault Handling in Up*/Down* Routed Networks with Multiple Roots
Ingebjorg Theiss and Olav Lysne, Simula Research Laboratory, Norway

Admission Control for DiffServ based Quality of Service in Cut-through Networks
Sven-Arne Reinemo, Frank Olaf Sem-Jacobsen, Tor Skeie, and Olav Lysne, Simula Research Laboratory, Norway

On Shortest Path Routing Schemes for Wireless Ad Hoc Networks
Subhankar Dhar, San Jose State University, USA, Michael Q. Rieck, Drake University, USA, Sukesh Pai, Microsoft Corporation, USA

A Hierarchical Routing Method for Load-Balancing
Sangman Bak, KTF, Korea

Ring based Routing Schemes for Load Distribution and Throughput Improvement in Multihop Cellular, Ad hoc and Mesh Networks
Gaurav Bhaya, B. S. Manoj, and C. Siva Ram Murthy, IIT Madras, India

2:45 pm - 4:45 pm
SESSION IV
Scientific and Engineering Applications
Chair: **Gagan Agrawal**
Ohio State University

A High Performance Computing Systems for Medical Imaging in the Remote Operating Room
(**Best Paper in Applications and Algorithms Area**)
Yasuhiro Kawasaki, Fumihiko Ino, Yasuharu Mizutani, Noriyuki Fujimoto, Toshihiko Sasama, and Yoshinobu Sato, Osaka University, Japan

Parallel Partitioning Techniques for Logic Minimization Using Redundancy Identification
B. Jayaram, A. Manoj Kumar, and V. Kamakoti, Indian Institute of Technology Madras, India

Parallel and Distributed Frequent Itemset Mining on Dynamic Datasets
Adriano Veloso, Matthew Eric Otey, and Srinivasan Parthasarathy, The Ohio State University, USA, Wagner Meira Jr., Universidade Federal de Minas Gerais, Brazil

A Volumetric FFT for Blue Gene/L
Maria Eleftheriou, Jose E. Moreira, Blake G. Fitch, and Robert S. Germain, IBM Thomas J. Watson Research Center, USA

A Nearly Linear-Time General Algorithm for Bi-Allele Haplotype Phasing
William Casey and Bud Mishra, New York University, USA

5:00pm - 7:00pm
INDUSTRY KEYNOTE SESSION
Chair: **Sudheendra Hangal**
SUN Microsystems

Friday Dec. 19

8:30 a.m - 9:30 a.m

KEYNOTE ADDRESS

"Energy Aware Algorithm Design via Probabilistic Computing: From Algorithms and Models to Moore's Law and Novel (Semiconductor) Devices"

Krishna V. Palem
Georgia Institute of Technology

10:00 a.m - noon

SESSION V

System Support in Overlay Networks, Clusters, and Grid

Chair: **Subhankar Dhar**
San José State University

Designing SANs to Support Low-Fanout Multicasts
Rajendra V. Boppana and Rajesh Boppana, University of Texas at San Antonio, USA, Suresh Chalasani, University of Wisconsin-Parkside, USA

POMA:Prioritized Overlay Multicast in Ad-hoc Environments
Abhishek Patil, Yunhao Liu, Lionel M. Ni, Li Xiao and Abdol-Hossein Esfahanian, Michigan State University, USA

Supporting Mobile Multimedia Services with Intermittently Available Grid Resources
Yun Huang and Nalini Venkatasubramanian, University of California, Irvine, USA

Exploiting Nonblocking Remote Memory Access Communication in Scientific Benchmarks on Clusters
Vinod Tipparaju, Manojkumar Krishnan, and Jarek Nieplocha, Pacific Northwest National Laboratory, USA, Gopalakrishnan Santhanaraman and D. K. Panda, Ohio State University, USA

10:00 a.m - noon

SESSION VI

Scheduling and Software Algorithms

Chair: **Rahul Garg**
IBM India

Scheduling Directed A-Cyclic Task Graphs on a Bounded Set of Heterogeneous Processors using Task Duplication
Christopher Dickinson and Sanjeev Baskiyar, Auburn University, USA

Double-Loop Feedback-Based Scheduling Approach for Distributed Real-Time Systems
Suzhen Lin and G. Manimaran, Iowa State University, USA

Combined Scheduling of Hard and Soft Real-Time Tasks in Multiprocessor Systems
B. Duwairi and G. Manimaran, Iowa State University, USA

An Efficient Algorithm to Detect Cycles in SPMD Programs
Manish P. Kurhekar, IBM India Research Lab, India, Rajkishore Barik, ETH Zentrum, Switzerland, Umesh Kumar, India Institute of Technology Delhi, India

Dynamic Load Balancing for I/O-Intensive Tasks on Heterogeneous Clusters
Xiao Qin, Hong Jiang, Yifeng Zhu, and David R. Swanson, University of Nebraska-Lincoln, USA

1:00 pm - 2:00 pm
KEYNOTE ADDRESS
"High Performance Computing Challenges in the Environmental Sciences"
Per Nyberg
Cray Inc.

2:00 pm - 2:30 pm
POSTER SETUP

2:30 pm - 5:00 pm
POSTER/PRESENTATION SESSION
This session will emphasize novel applications of high performance computing. It will offer a brief presentation time for each poster followed by a walk-up and talk setting.

For submission details, contact the poster/presentation chair:
Rajkumar Buyya, The University of Melbourne.(**rajkumar@buyya.com**)

6:30 pm - 9:30 pm
BANQUET AND CULTURAL PROGRAM
Speaker: Ketan Sampat, President, Intel India

Saturday Dec. 20

8:30 a.m. - 9:30 a.m.
KEYNOTE ADDRESS
"Standards Based High Performance Computing"
David Scott
Intel Corporation

10:00 a.m. - noon
SESSION VII
Network Design and Performance Issues
Chair: **Rajendra Boppana**
University of Texas at San Antonio

Delay and Jitter Minimization in High Performance Internet Computing
Javed I. Khan and Seung S. Yang, Kent State University, USA

An Efficient Heuristic Search for Optimal Wavelength Requirement in Static WDM Optical Networks
Swarup Mandal and Debashis Saha, Indian Institute of Management Calcutta, India, Sahadeb Jana, Maheshtala College, India

Slot Allocation Schemes for Delay Sensitive Traffic Support in Asynchronous Wireless Mesh Networks
V. Vidhyashankar, B. S. Manoj, and C. Siva Ram Murthy, Indian Institute of Technology Madras, India

Multi-Criteria Network Design using Evolutionary Algorithms
D Rajeev Kumar, Indian Institute of Technology Kharagpur, India

10:00 a.m. - noon
SESSION VIII
Grid Applications and Architecture Support
Chair: **Vipin Chaudhary**
Wayne State University

GridOS: Operating System Services for Grid Architectures
Pradeep Padala and Joseph N. Wilson, University of Florida, USA

Hierarchical and Declarative Security for Grid Applications
Isabelle Attali, Denis Caromel, and Arnaud Contes, University Nice Sophia Antipolis, France

Discover Middleware Substrate for Integrating Services on the Grid
Viraj N. Bhat and Manish Parashar, Rutgers, The State University of New Jersey, USA

Performance Analysis of a Hybrid Overset Multi-Block Application on Multiple Architectures
M. Jahed Djomehri, Computer Sciences Corporation, Rupak Biswas, NASA, USA

Complexity Analysis of a Cache Controller for Speculative Multithreading Chip Multiprocessors
Yoshimitsu Yanagawa, The Institute of Space and Astronautical Science, Japan, Luong Dinh Hung, Chitaka Iwama, Niko Demus Barli, Shuichi Sakai, and Hidehiko Tanaka, The University of Tokyo, Japan

1:00 a.m. - 2:00 a.m.
KEYNOTE ADDRESS
"One Chip, One Server: How do we Exploit its Power?"
Per Stenstrom
Chalmers University of Technology, Sweden

2:30 pm - 4:30 pm

SESSION IX
Performance Evaluation and Analysis
Chair: **Krishnaiya Thulasiraman**
University of Oklahoma

Data Locality Optimization for Synthesis of Efficient Out-of-Core Algorithms
(**Best Paper in Systems Area**)
Sandhya Krishnan, Sriram Krishnamoorthy, Gerald Baumgartner, Daniel Cociorva, Chi-Chung Lam, and P. Sadayappan, The Ohio State University, USA, J. Ramanujam, Louisiana State University, USA, David E. Bemholdt and Venkatesh Choppella, Oak Ridge National Laboratory, USA

Performance Evaluation of Working Set Scheme for Location Management in PCS Networks/Location Database Hierarchy Optimization for PCS Networks: A Genetic Algorithm Approach
Pravin Amrut Pawar Thadomal Shahani Engineering College, India, S. L. Mehdiratta, Indian Institute of Technology, India

Parallel Performance of the Interpolation Supplemented Lattice Boltzmann Method
C. Shyam Sunder, G. Baskar, and V. Babu, Indian Institute of Technology, India, David Strenski, Cray Inc., USA

Crafting Data Structures: A Study of Reference Locality in Refinement-Based Path Finding
Robert Niewiadomski, Jose Nelson Amaral, and Robert C. Holte, University of Alberta, Canada

Improving Performance Analysis using Resource Management Information
Tiago C. Ferreto, Research Center in High Performance Computing, Brazil, Cesar A. F. De Rose, Catholic University of Rio Grande do Sul, Brazil

2:30 pm - 4:30 pm

SESSION X
Scheduling and Migration
Chair: **Baba C. Vemuri**
University of Florida

Optimizing Dynamic Dispatches through Type Invariant Region Analysis
Mark Leair and Santosh Pande, Georgia Institute of Technology, USA

Thread Migration/Checkpointing for Type-Unsafe C Programs
Hai Jiang and Vipin Chaudhary, Wayne State University, USA

Web Page Characteristics-Based Scheduling
Yianxiao Chen and Shikharesh Majumdar, Carleton University, Canada

Controling Kernel Scheduling from User Space: An Approach to Enhancing Applications' Reactivity to I/O Events
Vincent Danjean and Raymond Namyst, Universite de Bordeaux, France

High-Speed Migration by Preemptive Mobility
Luk Stoops, Karsten Verelst, Tom Mens, and Theo D'Hondt, Vrije Universiteit Brussel, Belgium