8th International Conference on High Performance Computing

ADVANCE PROGRAM

December 17-20, 2001 • Hyderabad, India

www.hipc.org

ACKNOWLEDGMENTS

THE ORGANIZING COMMITTEE OF HiPC 2001 GRATEFULLY ACKNOWLEDGES THE SUPPORT AND PARTICIPATION OF THE FOLLOWING ORGANIZATIONS:

MAJOR SPONSORS

Hewlett Packard (India) Pvt. Limited
IBM (India) Limited
Indian Institute of Information Technology, Hyderabad
Infosys Technologies Limited, India
Microsoft Research
Satyam Computer Services Limited
Tata Consultancy Services

SPONSORS

Centre for Development of Advanced Computing, India
Compaq Computer Corporation (India) Pvt. Limited
Intel Innovation in Education
Silicon Graphics Systems (India) Pvt. Limited

SUPPORTING ORGANIZATIONS

Indian Institutes of Technology
Software Technology Parks of India
Tata Institute of Fundamental Research (TIFR), India

TABLE OF CONTENTS

CONFERENCE SITE

December 17
- Indian Institute of Information Technology, Hyderabad

December 18, 19, and 20
- Taj Krishna

(details on inside back cover)

ORGANIZATION

GENERAL CO-CHAIRS
Viktor K. Prasanna
University of Southern California

Sriram Vajapeyam
Consultant

VICE GENERAL CHAIR
Sajal K. Das
The University of Texas at Arlington

PROGRAM CHAIR
Burkhard Monien
Universität Paderborn, Germany

PROGRAM VICE-CHAIRS
Algorithms
Bruce M. Maggs
Carnegie Mellon University

Applications
Horst D. Simon
NERSC, Lawrence Berkeley National Laboratory

Architecture
Allan Gottlieb
New York University and NEC Research

Communication Networks
Cauligi S. Raghavendra
University of Southern California

Systems Software
Guang R. Gao
University of Delaware

PROGRAM COMMITTEE

ALGORITHMS
Micah Adler, University of Massachusetts, Amherst
Richard Anderson, University of Washington
John Byers, Boston University
Ramesh Hariharan, Indian Institute of Science
Michael Mitzenmacher, Harvard University
S. Muthukrishnan, AT&T Research
Stephane Perennes, INRIA
Sushil K. Prasad, Georgia State University
Rajmohan Rajaraman, Northeastern University
Andrea Richa, Arizona State University
Christian Scheideler, Johns Hopkins University
Assaf Schuster, Technion-Israel Institute of Technology

APPLICATIONS
Patrick Amestoy, ENSEEIHT-IRIT, Toulouse
Rupak Biswas, NASA Ames Research Center
Alvaro Coutinho, COPPE, Rio de Janeiro
Chris Ding, NERSC, Lawrence Berkeley National Laboratory
Jack Dongarra, Innovative Computing Lab, University of Tennessee
Robert Harrison, Pacific Northwest National Laboratory
Steve Jardin, Princeton Plasma Physics Laboratory
Ken Miura, Fujitsu, Japan
Franz-Josef Pfreundt, ITWM, Universität Kaiserslautern
Thomas Zacharia, Oak Ridge National Laboratory

ARCHITECTURE
Alan Berenbaum, Agere Systems
Doug Burger, University of Texas at Austin
Vijay Karamcheti, New York University
Gyungho Lee, Iowa State University
Daniel Litaize, Institut de Recherche en Informatique de Toulouse
Vijaykrishnan Narayanan, Pennsylvania State University
Yale Patt, University of Texas at Austin
Shuichi Sakai, University of Tokyo
Jaswinder Pal Singh, Princeton University
Mateo Valero, Universidad Politecnica de Catalunya
Sudhakar Yalamanchili, Proceler Inc.

COMMUNICATION NETWORKS
Ian F. Akyildiz, Georgia Institute of Technology
Hari Balakrishnan, MIT
Joseph Bannister, University of Southern California/ISI
Deborah Estrin, University of California, Los Angeles/ISI
Ramesh Govindan, University of Southern California/ISI
Anurag Kumar, Indian Institute of Science
T. V. Lakshman, Lucent Technologies
Masayuki Murata, Osaka University
Marco Ajmone Marsan, Politechnico de Torino
Douglas Maughan, DARPA ITO
K. G. Shin, University of Michigan

SYSTEMS SOFTWARE
Pradeep Dubey, IBM India Research Lab
R. Govindarajan, Indian Institute of Science
Wen-mei Hwu, University of Illinois at Urbana-Champaign
Laxmikant Kale, University of Illinois at Urbana-Champaign
Bernard Lecussan, SupAero, Toulouse
Yoichi Muraoka, Waseda University, Tokyo
Keshav Pingali, Cornell University
Martin Rinard, MIT Lab for Computer Science
Vivek Sarkar, IBM T. J. Watson Research Center
V. C. Sreedhar, IBM T. J. Watson Research Center
Theo Ungerer, Universität Karlsruhe

KEYNOTE CHAIR
Vipin Kumar
AHPCRC, University of Minnesota

POSTER/PRESENTATION CHAIR
Sartaj Sahni
University of Florida

TUTORIALS CHAIR
Manavendra Misra
KBkids.com

INDUSTRY LIAISON CHAIR
Sudheendra Hangal
Sun Microsystems

SCHOLARSHIPS CHAIR
Dheeraj Sanghi
Indian Institute of Technology, Kanpur

AWARDS CHAIR
Arvind
MIT

FINANCE CO-CHAIRS
A. K. P. Nambiar
Software Technology Park, Bangalore

Ajay Gupta
Western Michigan University

PUBLICITY CHAIR
Sandhya Dwarkadas
University of Rochester

LOCAL ARRANGEMENTS CHAIR
Kamal Karlapalem
Indian Institute of Information Technology, Hyderabad

PUBLICATIONS CHAIR
Nalini Venkatasubramanian
University of California at Irvine

STEERING CHAIR

Viktor K. Prasanna
University of Southern California

STEERING COMMITTEE

Jose Duato, Universidad Politecnica de Valencia
Viktor K. Prasanna, University of Southern California, Chair
N. Radhakrishnan, US Army Research Lab
Sartaj Sahni, University of Florida
Assaf Schuster, Technion-Israel Institute of Technology

NATIONAL ADVISORY COMMITTEE

R. K. Bagga, DRDL, Hyderabad
N. Balakrishnan, SERC, Indian Institute of Science
Ashok Desai, Silicon Graphics Systems (India) Pvt. Limited
Kiran Deshpande, Mahindra British Telecom Limited
H. K. Kaura, Bhabha Atomic Research Centre
Hans H. Krafka, Siemens Communication Software Limited
Ashish Mahadwar, Planetasia Limited
Susanta Misra, Motorola India Electronics Limited
Som Mittal, Digital Equipment (India) Limited
B. V. Naidu, Software Technology Park, Bangalore
N. R. Narayana Murthy, Infosys Technologies Limited
S. V. Raghavan, Indian Institute of Technology, Madras
V. Rajaraman, Jawaharlal Nehru Centre for Advanced Scientific Research
S. Ramadorai, Tata Consultancy Services, Mumbai
K. Ramani, Future Software Pvt. Limited
S. Ramani, Silverline Technologies Limited
Karthik Ramarao, Hewlett-Packard (India) Pvt. Limited
Kalyan Rao, Satyam Computers Limited
S. B. Rao, Indian Statistical Institute
H. Ravindra, Cirrus Logic
Uday S. Shukla, IBM Global Services India Pvt. Ltd
U. N. Sinha, National Aerospace Laboratories

WORKSHOP ORGANIZERS

Workshop on Embedded Systems

CO-CHAIRS
S. Jagannathan
Infineon Technologies

Santosh Pande
Georgia Institute of Technology

Workshop on Cutting Edge Computing

CO-CHAIRS
Uday S. Shukla
IBM Global Services India Pvt. Limited

Rajendra K. Bera
IBM Global Services India Pvt. Limited

Workshop on Bioinformatics and Computational Biology

CO-CHAIRS
Srinivas Aluru
Iowa State University

M. Vidyasagar
Tata Consultancy Services

SCHEDULE

	MONDAY	TUESDAY	WEDNESDAY	THURSDAY
7:30 am		Breakfast		
8:30 am		Opening Remarks		
9:00 am	Tutorial 1 Tutorial 2 Tutorial 3 Tutorial 4	Keynote Address	Keynote Address	Keynote Address
10:00 am	Embedded Computing Workshop (WS-I) & Cutting Edge Computing Workshop (WS-II)	Break	Break	Break
11:00 am		Technical Session I	Technical Session III	Technical Session V
noon		Lunch	Lunch	Lunch
1:00 pm	Lunch	Keynote Address	Technical Session IV	Keynote Address
2:00 pm	Tutorial 5 Tutorial 6 Tutorial 7 Tutorial 8	Break	Break	Break
3:00 pm	WS-I & WS-II (cont'd) & Bioinformatics and Computational Biology Workshop (WS-III)	Technical Session II	Industrial Track Session	Invited Session
4:00 pm		Break		
5:00 pm		Poster Session		
6:00 pm				
7:00 pm	Registration desk will be open from 7:30 am to 6:00 pm on Monday and from 8:00 am to 4:00 pm on Tuesday, Wednesday, and Thursday. Exhibits will be open from 10:00 am to 6:00 pm on Tuesday and Wednesday.	Conference Banquet, Cultural Program, and Dinner	Conference Banquet, Cultural Program, and Dinner	Conference registration fee includes breakfast, lunch, and refreshments on 17, 18, 19, and 20 December. It also includes the banquets on 18 and 19 December. **Conference site** December 17 Indian Institute of Information Technology, Hyderabad December 18, 19, and 20 Taj Krishna
8:00 pm				
9:00 pm				
10:00 pm				

OVERVIEW

KEYNOTE SPEAKERS

William Gropp
Argonne National Laboratory
"Whither MPI: Lessons From and the Future of MPI"

Masaru Kitsuregawa
University of Tokyo
"Parallel Web Mining"

Vivek Sarkar
IBM T. J. Watson Research Center
"High-Performance Scalable Java Virtual Machines"

Howard Jay Siegel
Colorado State University
"Heterogeneous Computing: Goals, Methods, and Open Problems"

Paul Spirakis
Computer Technology Institute of Greece
"Instability of FIFO and of Mixings of Stable Policies for Networks"

CONTRIBUTED PAPERS

There will be 29 contributed papers from 18 countries, chosen from 108 papers submitted in response to the call for papers. Contributed papers will be presented in 5 sessions.

INVITED PAPERS

Leading researchers will share their visions for networking and communications through invited papers to be presented in a plenary session titled "Advances and Research Challenges in Networking".

Organizer
Cauligi S. Raghavendra
University of Southern California

WORKSHOPS

Workshop on Embedded Computing

Workshop on Cutting Edge Computing

Workshop on Bioinformatics and Computational Biology

TUTORIALS

Designing Distributed Applications using Mobile Agents
Sridhar Iyer and Vikram Jamwal,
Indian Institute of Technology, Bombay

Opportunities and Challenges in Computational Biology
Srinivas Aluru, Iowa State University and
M. Vidyasagar, Tata Consultancy Services

The Bluetooth Technology: Specifications and Performance
Rajeev Shorey and Apurva Kumar,
IBM India Research Laboratory

Itanium Architecture and Compiler Optimizations
K. Muthukumar, Intel Technology India Pvt. Limited

Neural Network Models for Speech and Image Processing
B.Yegnanarayana, Indian Institute of Technology, Madras

QoS Support in Internet and Web Servers
Prasant Mohapatra, University of California, Davis

High Performance CORBA
Shikharesh Majumdar, Carleton University

Agent Teams
Milind Tambe, University of Southern California

POSTER/PRESENTATION SESSION

A plenary poster/presentation session emphasizing novel applications of high performance computing will be held on Tuesday, December 18. It will offer a brief presentation time for each poster followed by a walk-up and talk setting.

For details, contact:
Sartaj Sahni
Department of Computer and Information Science
CSE 301, University of Florida
Gainesville, FL 32611, USA
Email: sahni@cise.ufl.edu

EXHIBITS AND ORGANIZATION/ COMPANY PRESENTATIONS

Academic institutions, R&D labs, and companies are encouraged to use stalls available at the meeting to display exhibits and/or to make informal poster presentations about their research projects, products/product roadmaps, research and development opportunities, etc.

INDUSTRY LIAISON CHAIR

Sudheendra Hangal
Sun Microsystems
Email: hangal@eng.sun.com

TUESDAY, DEC. 18 KEYNOTES & TECHNICAL SESSIONS

8:30 am - 8:40 am

OPENING REMARKS

Viktor K. Prasanna
Sriram Vajapeyam
Burkhard Monien

8:40 am - 9:40 am

KEYNOTE ADDRESS

"Instability of FIFO and of Mixings of Stable Policies for Networks"
Paul Spirakis
Computer Technology Institute of Greece

Paul Spirakis obtained his Ph. D. from Harvard University in 1982. He became a full Professor at the University of Patras, Greece in 1990. He is currently the director of the Computer Technology Institute of Greece. He won the top prize of the Greek Math Association in 1973, and is a Distinguished Visiting Scientist of Max Planck Informatik.

His research interests include probabilistic algorithms, parallel and distributed algorithms and network protocols, exact analysis of algorithms, algorithms for mobile computing, and experimental algorithms as well as complexity of problems. He is a member of the Council of EATCS, the Greek representative in the European Union for Information Society and a consultant to the Greek State, the EU as well as to major Greek firms in Informatics. He is a member of scientific program or steering committees of the major conferences in his field. He is also a member of ACM, EATCS, Math Society of America, and the Greek Computer Society.

10:00 am - noon

SESSION I

Algorithms
Chair: J. L.V. Lewandowski
Princeton University

Mesh Algorithms for Multiplication and Division
S. Rao Kosaraju, The Johns Hopkins University

Compact Routing in Directed Networks with Stretch Factor of Two
Punit Chandra and Ajay Kshemkalyani,
University of Illinois at Chicago

Parametric Scheduling - Algorithms & Complexity
K. Subramani, West Virginia University,
Morgantown

An Efficient Algorithm for Computing Lower Bounds on Time and Processors for Scheduling Precedence Graphs on Multicomputer Systems
B. S. Panda, University of Hyderabad and
Sajal K. Das, University of Texas at Arlington

On Job Scheduling for HPC-Clusters and the dynP Scheduler
Achim Streit, University of Paderborn

An Adaptive Scheme for Fault-Tolerant Scheduling of Soft Real-Time Tasks in Multiprocessor Systems
R. Al-Omari, Arun K. Somani, and
G. Manimaran, Iowa State University

TUESDAY, DEC. 18

KEYNOTES & TECHNICAL SESSIONS

1:00 pm - 2:00 pm

KEYNOTE ADDRESS

"Whither MPI: Lessons From and the Future of MPI"

William Gropp
Argonne National Laboratory

William Gropp received Ph. D. in Computer Science from Stanford University in 1982. He is a Senior Computer Scientist and Associate Director of the Mathematics and Computer Science Division at Argonne, a Senior Scientist in the Dept. of Computer Science at the University of Chicago, and a senior fellow in the Argonne-University of Chicago Computation Institute. His research interests are in parallel computing, software for scientific computing, and numerical methods for partial differential equations. Dr. Gropp has played a major role in the development of the MPI message-passing standard. He is co-author of MPICH, the most widely used implementation of MPI, and was involved in the MPI Forum as a chapter author for both MPI-1 and MPI-2. He has written many books and papers on MPI, including "Using MPI" and "Using MPI-2". Dr. Gropp is also one of the designers of the PETSc parallel numerical library and has developed efficient and scalable parallel algorithms for the solution of linear and nonlinear equations. In addition, he is involved in several other advanced computing projects, including performance modeling, data structure modification for ultra-high-performance computers, and development of component-based software to promote interoperability among numerical toolkits.

2:15 pm - 4:15 pm

SESSION II

Applications

Chair: P. J. Narayanan
Indian Institute of Information Technology, Hyderabad

Gyrokinetic Simulations of Plasma Turbulence on Massively Parallel Computers
J. L. V. Lewandowski, Z. Lin, W. W. Lee, T. S. Hahm, and W.M. Tang, Princeton University

A Parallel Krylov-type Method for Nonsymmetric Linear Systems
Anthony T. Chronopoulos, University of Texas, San Antonio and Andrey B. Kucherov, Moscow State University

Evolving Cellular Automata Based Associative Memory for Pattern Recognition
Niloy Ganguly, IISWBM, Calcutta and Arijit Das, Pradipta Maji, Biplab K. Sikdar, and P. Pal Chaudhuri, Bengal Engineering College

Efficient Parallel Algorithms and Software for Compressed Octrees with Applications to Hierarchical Methods
Bhanu Hariharan and Srinivas Aluru, Iowa State University

A Case Study of Improving Memory Locality In Polygonal Model Simplification: Metrics and Performance
Victor Salamon and Paul Lu, University of Alberta, Ben Watson and Dima Brodsky, Northwestern University and Dave Gomboc, The University of British Columbia

4:30 pm - 6:30 pm

POSTER/PRESENTATION SESSION

This session will emphasize novel applications of high performance computing. It will offer a brief presentation time for each poster followed by a walk-up and talk setting. For submission details, contact:

Chair: Sartaj Sahni
Email: sahni@cise.ufl.edu

7:00 pm - 10:00 pm

BANQUET AND CULTURAL PROGRAM

WEDNESDAY, DEC. 19 KEYNOTES & TECHNICAL SESSIONS

8:30 am - 9:30 am

KEYNOTE ADDRESS

"High-Performance Scalable Java Virtual Machines"
Vivek Sarkar
IBM T. J. Watson Research Center

Vivek Sarkar is a Research Staff Member and Senior Manager of the Programming Technologies department at the IBM T. J. Watson Research Center. The projects in his department span the areas of dynamic compilation, adaptive optimization, high-performance Java virtual machines, component verification, debugging of multithreaded programs, software configuration management, and XML technologies for database applications.

Dr. Sarkar joined IBM in 1987, after obtaining a Ph. D. from Stanford University. During 1998 to 2000, he led the Jalapeno optimizing compiler group at the IBM T. J. Watson Research Center in building a new dynamic optimizing compiler for Java. He has been a member of the IBM Academy of Technology since 1995.

10:00 am - noon

SESSION III

Architecture
Chair: Sriram Vajapeyam
Consultant

Shared Virtual Memory Clusters with Next-Generation Interconnection Networks and Wide Compute Nodes
Courtney R. Gibson and Angelos Bilas,
The University of Toronto

Stream-Packing: Resource Allocation in Web Server Farms with a QoS Guarantee
Johara Shahabuddin, IBM India Research Lab., Abhay Chrungoo, Indian Institute of Technology, Guwahati, Vishu Gupta, Sandeep Juneja, and Sanjiv Kapoor, Indian Institute of Technology, Delhi, and Arun Kumar, IBM India Research Lab.

Weld: A Multithreading Technique towards Latency-tolerant VLIW Processors
Emre Ozer and Thomas M. Conte,
North Carolina State University

Putting Data Value Predictors to Work in Fine-Grain Parallel Processors
Aneesh Aggarwal and Manoj Franklin,
University of Maryland

Confidence Estimation for Branch Prediction Reversal
Juan L. Aragón, José González, and José M. García, Universidad de Murcia, and Antonio González, Universitat Politecnica de Catalunya

Retargetable Program Profiling Using High Level Processor Models
Rajiv Ravindran and Rajat Moona,
Indian Institute of Technology, Kanpur

WEDNESDAY, DEC. 19 — KEYNOTES & TECHNICAL SESSIONS

1:00 pm - 3:00 pm

SESSION IV

Systems Software

Chair: Guang R. Gao
University of Delaware

Towards Automatic Synthesis of High-Performance Codes for Electronic Structure Calculations: Data Locality Optimization
Daniel Cociorva, John W. Wilkins, Gerald Baumgartner, and P. Sadayappan, The Ohio State University, J. Ramanujam, Louisiana State University, Marcel Nooijen, Princeton University, David E. Bernholdt, Oak Ridge National Laboratory, and Robert Harrison, Pacific Northwest National Laboratory

Block Asynchronous I/O - An Infrastructure for High-Performance User-Level Filesystems
Muthian Sivathanu, Venkateshwaran Venkataramani, and Remzi H. Arpaci-Dusseau, University of Wisconsin, Madison

TWLinuX: Operating System Support for Optimistic Parallel Discrete Event Simulation
Subramania Sharma T. and Matthew J. Thazhuthaveetil, Indian Institute of Science

Low-Cost Garbage Collection for Causal Message Logging with Independent Checkpointing
Jinho Ahn and Chong Sun Hwang, Korea University, Seoul

Improving the Precise Interrupt Mechanism of Software Managed TLB Miss Handlers
Aamer Jaleel and Bruce Jacob, University of Maryland

Hidden Costs in Avoiding False Sharing in Software DSMs
K. V. Manjunath and R. Govindarajan, Indian Institute of Science

3:15 pm - 6:30 pm

INDUSTRIAL TRACK SESSION

(TBD)

7:00 pm - 10:00 pm

BANQUET AND CULTURAL PROGRAM

THURSDAY, DEC. 20

KEYNOTES & TECHNICAL SESSIONS

8:30 am - 9:30 am

KEYNOTE ADDRESS

"Heterogeneous Computing: Goals, Methods, and Open Problems"

Howard Jay Siegel
Colorado State University

H. J. Siegel is the Abell Distinguished Professor of Electrical and Computer Engineering at Colorado State University. From August 1976 to August 2001, he was a Professor in the School of Electrical and Computer Engineering at Purdue University. He received two B. S. degrees from the Massachusetts Institute of Technology (MIT), and the M. A., M. S. E., and Ph. D. degrees from Princeton University.

Dr. Siegel has co-authored over 280 published technical papers in the areas of parallel and distributed computing. He was a Coeditor-in-Chief of the Journal of Parallel and Distributed Computing, and was on the Editorial Boards of the IEEE Transactions on Parallel and Distributed Systems and the IEEE Transactions on Computers. He is a Fellow of the IEEE and a Fellow of the ACM.

10:00 am - noon

SESSION V

Communication Networks

Chair: Joseph Bannister
University of Southern California/ISI

Load Balancing in Cellular Networks: How Much We Can Achieve
Swades K. De and Sajal K. Das, University of Texas at Arlington

Performance Evaluation of Mobile Agents for E-Commerce Applications
Rahul Jha and Sridhar Iyer, Indian Institute of Technology, Bombay

Performance Evaluation of Real-Time Communication Services on High-Speed LANs under Topology Changes
J. Fernández and J. M. García, Universidad de Murcia, and J. Duato, Universidad Politecnica de Valencia

Wavelength Conversion Placement and Wavelength Assignment in WDM Optical Networks
Mahesh Sivakumar and Suresh Subramaniam, The George Washington University

Identifying Long-Term High-Bandwidth Flows at a Router
Smitha, Inkoo Kim, and A. L. Narasimha Reddy, Texas A & M University, College Station

Variable Length Packet Switches: Input Queued Fabrics with Finite Buffers, Speedup and Parallelism
D. Manjunath and B. Sikdar, Rensselaer Polytechnic Institute

1:00 pm - 2:00 pm

KEYNOTE ADDRESS

"Parallel Web Mining"

Masaru Kitsuregawa
University of Tokyo

Masaru Kitsuregawa received the Doctor of Engineering degree in Information Engineering from the University of Tokyo in 1983. In 1983, he joined the Institute of Industrial Science (IIS) at the University of Tokyo as a lecturer. He is currently a Professor and a Director of the Center for Conceptual Information Processing Research, IIS, University of Tokyo. His research has been directed toward the design of 100 node, highly parallel PC cluster system for performance database/data mining systems. His current research interest is web mining. He has published more than 150 refereed papers. He serves as a trustee member of the VLDB Endowment, as an Asian Coordinator of the IEEE TCDE, and is the chairperson of ACM SIGMOD Japan Chapter. Dr. Kitsuregawa has served as the chairperson of SIGDE of IEICE Japan. He was a general chair of PAKDD2000 and a member of Steering Committee of IEEE ICDE and PAKDD. He is currently the editor of IEEE TKDE Journal.

2:15 pm - 4:15 pm

INVITED SESSION

Advances and Research Challenges in Networking

Chair: Cauligi S. Raghavendra
University of Southern California

Modeling and Simulation of Complex Systems: Networks and Biological Systems
Sri Kumar, Defense Advanced Research Projects Agency, USA

An Optical Booster for Internet Routers
Joseph Bannister, University of Southern California/ISI

Intelligent, Model Based Network Engineering
Anurag Kumar, Indian Institute of Science

Performance Analysis of Data Services over GPRS
Marco Marsan, Marco Gribaudo, Michela Meo, and Matteo Sereno, Politechnico di Torino

Trends in Architectures and Technologies for QoS Preserving Packet Switch Fabrics
Vijay Kumar, Lucent Technologies

MONDAY, DEC. 17

WORKSHOPS & TUTORIALS

9:00 am - 6:30 pm

WORKSHOP I

Workshop on Embedded Systems

Embedded systems are finding increasing use in diverse and demanding application domains and research challenges are encountered for achieving desired level of performance goals in those application domains. This workshop will provide a forum to discuss latest research both in academia and industry and to explore new directions. In addition to contributed papers, we plan to have an industrial panel and invited talks by leading researchers and technocrats in the field.

Topics of interest include but are not limited to:
- Algorithms and Software Design
- Emerging Application Domains
- Compiler Optimization for Embedded Systems
- System Software for Embedded Systems
- Embedded Processor Architectures and Trends
- Embedded Signal Processing

Submission guidelines

Papers reporting both new research as well as comprehensive experiences and evaluation of systems are welcome. To submit an original research paper, send your complete manuscript not exceeding 5 pages including figures. Submissions should be sent as a single e-mail message to both the workshop co-chairs. Submissions should be in postscript form, which must be interpretable by ghost script. The postscript must use standard fonts, or include the necessary fonts, and must be prepared for (US Letter 8.5"x11") or A4 page sizes. All papers will be reviewed by the program committee.

Important dates

September 01, 2001:
Workshop paper due

October 01, 2001:
Author notification

November 01, 2001:
Final papers due

ORGANIZERS

S. Jagannathan
Infineon Technologies
10th Floor, Discoverer
International Tech Park
Whitefield Road
Bangalore -560066, India
Tel: +91-80-841-0017/18 ext 2073
Fax: +91-80-841-0012
Email: sjagan@ieee.org

Santosh Pande
College of Computing
Georgia Institute of Technology
801 Atlantic Drive
Atlanta, GA 30332 USA
Tel: +1-404-385-2169
Fax: +1-404-385-2295
Email: santosh@cc.gatech.edu

Advisory Committee

Kanaka Kripakaran
Siemens Information Systems Ltd.

Suthikshn Kumar
Infineon Technologies

Vivek S. Nittoor
Sanyo LSI Tech India

For more information visit
http://www.hipc.org/hipc2001/

9:00 am - 6:30 pm

WORKSHOP II

Workshop on Cutting Edge Computing

This workshop will feature invited presentations from experts in such areas as Quantum Computing, Supercomputing/Deep Computing, Datamining of Scientific Data, etc. The goal is to bring to the attention of researchers and practitioners, recent R&D advances in computing technologies that are expected to dominate the future of computing.

Topics of interest include but are not limited to:
- Supercomputing/Deep Computing
- Quantum Computing
- Advanced Algorithms
- Datamining of Scientific Data

For further information contact the organizers.

ORGANIZERS

Uday S. Shukla
Director
IBM Global Services India, Exports
Email: ushukla@in.ibm.com

Rajendra K. Bera
Head, R&D (Exports Services)
IBM Global Services India Pvt. Ltd
Golden Enclave, Airport Road
Bangalore 560017, India
Tel: +1-91-80-526-2355 ext 2540
Fax: +1-91-80-527-7374
Email: rbera@in.ibm.com

For more information visit
http://www.hipc.org/hipc2001/

MONDAY, DEC. 17

2:00 pm - 6:30 pm

WORKSHOP III

Workshop on Bioinformatics and Computational Biology

Discovery of biomolecular sequences and their relation to the functioning of organisms has created a number of challenging problems for computer scientists, and has led to the emerging interdisciplinary field of bioinformatics and computational biology. The field holds immense potential for aiding in future discoveries such as the design of proteins for efficient administering of drugs and personalized medicine.

The goal of this workshop is to provide a forum for researchers and practitioners to discuss recent research and developments in bioinformatics and computational biology. The workshop will include contributed papers and invited talks.

Topics of interest include but are not limited to:
- Bioinformatic databases
- Computational genomics
- Computational proteomics
- DNA assembly, clustering, and mapping
- Gene expression and microarrays
- Gene identification and annotation
- Molecular evolution
- Molecular sequence analysis
- Protein structure

Submission Guidelines

Papers reporting on original research (both theoretical and experimental) in all areas of bioinformatics and computational biology are sought. Surveys of important recent results and directions are also welcome. To submit a paper, send a postscript copy of the paper by email to either of the workshop co-chairs. The paper should not exceed 10 single-spaced pages (US Letter or A4 size) in 11pt font or larger. All papers will be peer-reviewed.

Important dates

September 15, 2001:
Workshop paper due

October 15, 2001:
Author notification

November 15, 2001:
Camera-ready paper due

ORGANIZERS

Srinivas Aluru
Dept. of Electrical & Computer Engg. and
Lawrence H. Baker Center for Bioinformatics
& Biological Statistics
Iowa State University
3218 Coover Hall
Ames, IA 50011 USA
Tel: +1-515-294-3539
Fax: +1-515-294-8432
Email: aluru@iastate.edu

M. Vidyasagar
Executive Vice President
Tata Consultancy Services
Coromandel House
1-2-10 Sardar Patel Road
Secunderabad 500 003, India
Tel: +91-40-626-0805
Fax: +91-40-781-4520
Email: sagar@atc.tcs.co.in

For more information visit
http://www.ee.iastate.edu/~aluru/bcb2001

9:00 am - 1:00 pm

TUTORIAL I

Designing Distributed Applications using Mobile Agents

Sridhar Iyer and Vikram Jamwal
Indian Institute of Technology, Bombay

Audience: This tutorial is intended for software architects, researchers, educators, and graduate students interested in building background in the area of mobile agents.

Course Description: This tutorial begins with exploring the need for new approaches to software design and introduces the basic concepts in the mobile agent technology. The tradeoffs in using a mobile agents based approach for designing distributed applications are discussed in detail.

Subsequently, issues in designing mobile agents frameworks are discussed, with a comparison of some popular frameworks such as Voyager, Aglets, and Concordia. This is followed by case studies of mobile agents based distributed applications, in domains such as e-commerce, workflow and distance education. The tutorial concludes with highlighting some open research issues in the area.

Lecturers: Sridhar Iyer is presently an Assistant Professor in the School of Information Technology at IIT, Bombay. Prior to this, he has been a faculty member in the Dept. of Computer Science & Engg. at IIT, Guwahati. He received his B. Tech, M. Tech, and Ph. D. from the Dept. of Computer Science & Engg. at IIT, Bombay. His current research interests include: mobile agents, ad hoc networking, and analysis of distributed programs.

Vikram Jamwal is presently a Ph. D. student in the School of Information Technology at IIT, Bombay. He received his M. Tech from IIT, Bombay. Prior to this, he has worked as a visiting scientist at the National Centre for Software Technology and as a Design Executive at Crompton Greaves Ltd. His current research interests include: mobile agents, design of large-scale distributed applications and distance education.

9:00 am - 1:00 pm

TUTORIAL II

Opportunities and Challenges in Computational Biology

Srinivas Aluru
Iowa State University
M. Vidyasagar
Tata Consultancy Services

Audience: This tutorial is meant for computer professionals, software developers, researchers, educators, graduate students, and employees from software companies interested in targeting computational biology as an application area.

Course Description: Computational biology is emerging as a major thrust area for academic research and industrial application in the 21st century. The goal of this tutorial is to provide a comprehensive introduction to the field of computational biology to an audience with a computing background that is interested in participating in research and/or commercial applications in this field. Major subareas in computational biology including sequence alignments, mapping, fragment assembly, microarray data analysis and protein folding will be covered in the tutorial. Current progress on genome-scale projects will be discussed and information on resources available on the internet including genomic and protein databases and software tools will be provided. Potential applications of high performance computing to computational biology will be highlighted. Important open problems and opportunities for development of software systems will be discussed. No background in biology is assumed.

Lecturers: Srinivas Aluru is an Associate Professor in the Dept. of Electrical and Computer Engg. and the Lawrence H. Baker Center for Bioinformatics and Biological Statistics at Iowa State University. He received his B. Tech degree in Computer Science from the Indian Institute of Technology, Madras, in 1989 and his M. S. and Ph. D. degrees in Computer Science from Iowa State University, in 1991 and 1994, respectively. He has held academic positions at New Mexico State University (1996 - 1999) and Syracuse University (1994 - 1996). His research interests include parallel algorithms and applications, computational biology, and scientific computing. He is a recipient of the NSF CAREER Award.

Mathukumalli Vidyasagar received the B. S., M. S., and Ph. D. degrees in Electrical Engineering from the University of Wisconsin in 1965, 1967, and 1969, respectively. He taught at Marquette University (1969-70), Concordia University (1970-80), and the University of Waterloo (1980-89). From 1989 to 2000, he served as the Director of the Centre for Artificial Intelligence and Robotics in Bangalore, India. In 2000, he took up his current assignment as Executive Vice President (Advanced Technology) in Tata Consultancy Services. He is the author or co-author of seven books and more than one hundred and twenty journal papers. He is a Fellow of IEEE, the Indian Academy of Sciences, the Indian National Science Academy, the Indian National Academy of Engineering, and the Third World Academy of Sciences. His current research interests are control theory, machine learning, and cryptography.

MONDAY, DEC. 17

9:00 am - 1:00 pm

TUTORIAL III

The Bluetooth Technology: Specifications and Performance

Rajeev Shorey and Apurva Kumar
IBM India Research Laboratory

Audience: This tutorial is intended for computer professionals, telecommunication engineers, researchers, educators, and graduate students interested in the Bluetooth technology.

Course Description: Bluetooth technology provides a low cost, low power, and low complexity solution for ad-hoc wireless connectivity. The technology is capable of connecting a wide variety of devices like Personal Digital Assistants (PDAs), mobile and cordless phones, headsets, desktops and notebook PCs, digital cameras, home appliances, etc. The applications include eliminating cables/ wires between devices like PCs, printers, modems, projectors, self synchronization between PDAs and PCs, wireless connection to local area networks (LANs) through access points and internet through mobile phones, providing home networking solutions, etc.

This tutorial will provide an overview of Bluetooth technology and its applications. The Bluetooth system will be introduced and various modes of operation will be discussed. A description of functionalities of Bluetooth layers and the protocol specifications will be presented. Various usage scenarios and the profiles which support them will be explained.

An insight into the performance of Bluetooth based systems will be provided. Means of evaluating/improving performance of Bluetooth based systems will be discussed. Key features of an open-source Bluetooth simulation tool which can be used to evaluate the performance of applications over Bluetooth will be described.

We will provide an overview of a number of open research problems related to Bluetooth specifically, and short range wireless in general. Some of the problems that we will discuss are MAC scheduling with and without low power modes, performance of TCP/UDP over a Bluetooth piconet and Bluetooth capacity.

Lecturers: Apurva Kumar received his M.S degree from the Indian Institute of Technology, New Delhi in 1997. From February, 1997 to August, 1999, he was with Silicon Automation Systems, Bangalore, where he was involved in wireless systems engineering projects with Nortel Networks. Since September, 1999, he is working as a Research Staff Member in IBM India Research Laboratory, New Delhi.

Rajeev Shorey received a Bachelor of Engineering (B.E) in Computer Science from the department of Computer Science and Automation, IISc, Bangalore, in 1987. He received the M. S and Ph. D degrees in Electrical Communication Engineering from the IISc, in 1990 and 1995 respectively. From December, 1995 to February, 1998, he was with Silicon Automation Systems, Bangalore, where he worked on the performance modeling and analysis of CDMA networks. Since March, 1998, he is a Research Staff Member in the IBM India Research Laboratory. Dr. Shorey has numerous papers in international journals and conferences to his credit. He has more than 9 IBM US patents that are pending and has been in the technical program committee of several international conferences in networking. He is also an adjunct faculty in the department of Computer Science and Engineering, IIT, New Delhi. Dr. Shorey is a senior member of the IEEE.

9:00 am - 1:00 pm

TUTORIAL IV

Itanium Architecture and Compiler Optimizations

K. Muthukumar
Intel Technology India Pvt. Limited

Audience: This tutorial is intended for computer professionals, compiler engineers, software developers, researchers, educators, and graduate students interested in learning about the Itanium(TM) architecture and state-of-the-art compiler technologies.

Course Description: Itanium(TM) is Intel's new 64-bit architecture. It is based on the EPIC (Explicitly Parallel Instruction Computing) concept which exploits the high level of Instruction Level Parallelism (ILP) found in application software. To accomplish this goal, Itanium provides a powerful set of features such as control and data speculation, predication, register rotation, loop branches, and a large register file. By using these features, the compiler plays a crucial role in achieving the overall performance of an Itanium platform. This tutorial describes the main features of the Itanium architecture and explains how the various optimization phases in the Intel production compiler for Itanium exploits these features. This will cover: (1) optimizations in the code generator such as predication, global code scheduling, software pipelining, and global register allocation, and (2) other optimizations such as loop unrolling, procedure inlining, inter-procedural analysis, loop-carried scalar replacement, array prefetches, and partial redundancy elimination.

This tutorial will help the participant appreciate the many novel features of Itanium, the opportunities they provide for exploiting ILP in application code, and how these have been exploited in a production compiler.

Lecturer: Dr. K. Muthukumar is an Engineering Manager at Intel India Technology Private Limited, Bangalore and a technical lead of the Itanium Compiler group in Santa Clara, California. He heads the Bangalore Compiler Lab at Intel. He has implemented several optimizations in the software-pipelining phase of the compiler. His interests are in compiler optimization, and computer architecture. Prior to joining Intel, he worked at IBM and Apple Computer. He obtained his B. Tech from IIT, Madras, M. S. from the Rensselaer Polytechnic Institute, and Ph. D. in Computer Science from the University of Texas at Austin. He has published many papers in the area of compiler optimization. He has submitted 6 patent applications related to his work on Itanium compiler technology.

2:00 pm - 6:00 pm

TUTORIAL V

Neural Network Models for Speech and Image Processing

B.Yegnanarayana
Indian Institute of Technology, Madras

Audience: Any one with an engineering degree, preferably Computer Science or Electrical Engineering, will find this course useful. It is also useful for any practicing engineer or a scientist in a research and development establishment and for teachers in academic institutions.

Course Description: Most applications involving speech and images require extraction of information in the form of features from raw data and use those features for classification, storage and retrieval of information. Conventional methods of signal processing use linear methods or some simple nonlinear methods. But in some cases the information is embedded in features which require complex nonlinear processing of the data for extraction. Moreover, many classification models require nonlinear dividing surfaces in the feature space. Models based on artificial neural networks have been found to be very powerful for feature extraction and classification. This tutorial presents basics of neural network models for feature extraction and classification. In particular, the higher order statistical feature extraction from data, distribution capturing ability, and combining evidence from several classifiers, will be discussed in detail. Some applications of these models for processing real speech and image data will be illustrated. In particular, applications for speech enhancement, speech recognition and speaker recognition/verification will be discussed to demonstrate the potential of nonlinear models for these applications. Applications in image processing include image compression, texture analysis and edge extraction, with particular reference to remotely-sensed multispectral data. The course will be self-contained. No specific background of speech and image processing is assumed. The lectures will be illustrated with demonstrations of some speech and vision systems.

Lecturer: B.Yegnanarayana is a Professor at IIT, Madras since 1980. Prior to joining IIT, he was a visiting Associate Professor of Computer Science at Carnegie Mellon University from 1977-1980. He was a member of the faculty at the Indian Institute of Science, Bangalore from 1966 to 1978. He did B. E., M. E., and Ph. D. from IISc, Bangalore, in 1964, 1966, and 1974, respectively. His research interests are in speech, image processing, and neural networks. He has published several papers in these areas in IEEE and other international journals. He is also the author of the book "Artificial Neural Networks", published by Prentice-Hall of India, in 1999. He is a Fellow of the Indian National Academy of Engineering and a Fellow of the Indian National Science Academy.

2:00 pm - 6:00 pm

TUTORIAL VI

QoS Support in Internet and Web Servers

Prasant Mohapatra
University of California, Davis

Audience: This tutorial is aimed at both researchers and practitioners. It will also immensely help students pursuing research in Internet and other networking issues.

Course Description: The current best-effort service model of the Internet and its servers are not suitable for growing applications such as continuous media, e-commerce, and other business services. To provide better services to these expanding classes of applications, it is necessary for the Internet infrastructure to provide QoS support. This tutorial targets QoS issues at both the network level as well as server level. The key techniques proposed for supporting QoS in the Internet include integrated services (IntServ), differentiated services (DiffServ), multiprotocol label switching (MPLS), and traffic engineering. We will discuss various issues involved in these techniques. To provide end-to-end QoS, Internet servers must also be capable of providing differentiated services. Resource management is the key issue in providing efficient service differentiation at the server level. Thus, we will analyze scheduling, admission control, and other implementation details.

In this tutorial, we will present the state-of-the-art issues on the proposed topic as well as introduce new and novel avenues for research and development. Future work on important issues like receiver-based DiffServ, multicasting, managing dynamic content on the web, and overload control will also be discussed.

Lecturer: Prasant Mohapatra received his Ph. D. in computer engineering from the Pennsylvania State University in 1993. He was with Iowa State University from 1993 to 1999. From 1999 to 2001, he was with the Dept. of Computer Science and Engg. at Michigan State University. From the Fall of 2001, he has been with the Dept. of Computer Science at the University of California, Davis. His research interests include computer networks, server and storage systems, and ad hoc networks. Dr. Mohapatra is a senior member of the IEEE and a member of the ACM. He is currently on the editorial board of the IEEE Transactions on Computers.

2:00 pm - 6:00 pm

TUTORIAL VII

High Performance CORBA

Shikharesh Majumdar
Carleton University

Audience: This tutorial is meant for researchers, system designers, users of CORBA-based systems and products, and graduate students. Some background in distributed processing is required. A minor background in CORBA is desirable but not essential.

Course Description: Heterogeneity is natural in systems built using the popular Distributed Object Computing (DOC) paradigm. Different system components in such systems often use different programming languages and operating systems. Middleware provides interoperability between clients and servers in such heterogeneous DOC systems. Common Object Request Broker Architecture (CORBA) is a middleware standard proposed by the Object Management Group (OMG). Most of the available commercial CORBA compliant middleware products provide inter-operability, but often incur a performance penalty. High scalability and low latency are crucial in many applications that include telecommunication products, process control systems, and other performance demanding applications. This tutorial will address these performance issues in CORBA-based systems. Three different classes of performance optimization techniques, guidelines for application design, adopting an appropriate client-middleware-server interaction architecture and techniques that exploit limited heterogeneity in systems will be described. Sample experimental results demonstrating their effectiveness will be discussed.

Lecturer: Shikharesh Majumdar is a Professor at the Dept. of Systems and Computer Engg. at Carleton University in Ottawa. He holds an M. Sc. and a Ph. D. degree in Computational Science from University of Saskatchewan, Saskatoon. Dr. Majumdar's research interests are in the areas of parallel and distributed processing, operating systems, and performance evaluation. He has authored over fifty technical papers, and has won a best presentation and a best paper award in two international IEEE conferences. He is the Associate Editor of the IEEE TC on Operating Systems Bulletin, and has served in the program and organizing committees of various international conferences. He is a member of the ACM and a Distinguished Visitor for the IEEE Computer Society.

2:00 pm - 6:00 pm

TUTORIAL VIII

Agent Teams

Milind Tambe
University of Southern California

Audience: Researchers, educators, practitioners, and graduate students with an interest in intelligent agents will benefit from this tutorial.

Course Description: Teamwork is a critical capability in a large number of multi-agent environments. For instance, in virtual environments for training and education, teamwork among agents is critical to provide the right environment for human trainees. Teamwork among software agents is crucial in applications that involve assistance to human organizations, as well as in information gathering, planning and logistics. Teamwork may also offer new methods for integrating heterogeneous software components. Finally, teamwork is obviously critical in distributed robotic applications as in future multi-spacecraft missions.

In this tutorial, I will survey the state of the art in agent teamwork. Fundamentally, this area has focused on enabling different autonomous entities (e.g., software agents or robots) to work together, using inspirations from human teamwork. Thus, researchers have been attempting to fundamentally understand the nature of teamwork and practical techniques to rapidly construct robust agent teams. One key lesson learned is that in complex, uncertain environments, creating fixed, domain-specific coordination plans to manage teamwork is highly problematic: these plans are not reusable across domains, and their lack of flexibility can lead to severe failures. Instead, a new approach based on developing a general teamwork model appears to provide more promise. These models enables agents to explicitly reason about commitments and responsibilities in teamwork, and flexibly plan own coordination. Furthermore, these models are reusable across domains, aiding rapid construction of agent teams. A key outcome of this work is the notion of "team-oriented programming" to enable developers to program agent teams at a high-level, while the coordination is automatically generated at run time due to the teamwork model.

Building on a similar tutorial delivered at the European Summer School on Agents, and classes on multi-agents taught at the University of Southern California's computer science department, this tutorial will first cover theory of teamwork and then practical teamwork models based on such theory. We will cover one particular teamwork model, called STEAM, in more detail. STEAM has been the basis of several agent teams that we have developed, including pilot teams for battlefield simulations, top-performing agent teams for RoboCup soccer, teams integrating software agents over the internet, and more recently, "Electric Elves", a team of software assistants that help researchers in their daily activities, operating 24/7 at ISI since 6/1/2000.

Lecturer: Milind Tambe is an Associate Professor of Computer Science at the University of Southern California (USC) and a project leader at USC's Information Sciences Institute (ISI). His research interests are in the areas of multi-agent systems, particularly, in topics such as teamwork, coordination, and negotiations and agent modeling. A member of the board of directors of the International Foundation for Multi-agent Systems, and a trustee of the RoboCup Federation, he is also on the editorial board of the Journal of Autonomous Agents and Multi-agent Systems, Journal of Artificial Intelligence Research, and IEEE Intelligent Systems. He has served as the program co-chair for the International Conference on Multi-agent Systems (ICMAS'2000), and as senior program committee member for the AAAI and Agents conferences. (http://www.isi.edu/teamcore/tambe)

LOCAL INFORMATION

Conference site
December 17

Indian Institute of Information
Technology, Hyderabad
Gachibowli
Hyderabad 500019, India
http://www.iiit.net

Tel: +91-40-3001413
Fax: +91-40-3001413

December 18, 19, and 20

Taj Krishna
Road No. 1
Banjara Hills
Hyderabad 500034, India

Tel: +91-40-666-2323
+91-40-339-2323
Fax: +91-40-666-1313
+91-40-666-3366

About Hyderabad
Hyderabad, known as the City of Pearls, is the fifth largest metropolitan city in India and is fast emerging as the hub of Information Technology in India. Many multi-national companies including Microsoft, Motorola, Oracle, GE Capital, and IBM, among others, have set up development units at Hyderabad. It is home to upcoming premier universities such as Indian Institute of Information Technology and Indian School of Business as well as to some of the oldest and most prestigious universities in India. Hyderabad is highly cosmopolitan and presents a mix of various cultures, which is reflected in its ethnic, cultural, architectural, and culinary diversity.

Sightseeing Tours
There will be two local sightseeing tours organized during the conference.

Tour 1 - December 20, 5:00 pm - 9:00 pm
Tour 2 - December 21, 8:00 am - 5:00 pm

Please check the HiPC website for details.

Travel Checklist

Visa:
All non-Indian-citizens are required to have an Indian visa to enter the country. Please allow yourself sufficient time (say 2-3 weeks) to procure an appropriate visa from your nearest Indian consulate. Please check the conference website for information about Indian consulates.

Flight Reservations:
Flights to India tend to fill up well ahead of the December holiday season. We recommend that you make your flight reservations about 3-4 months in advance.

Vaccinations (shots):
Many first-time travelers to India prefer to get preventive vaccinations.

Foreign Exchange:
While international credit cards are widely accepted in commercial establishments in India, several places rely on cash transactions in the local currency (Indian Rupee). We suggest that you carry some Indian currency when entering India or buy Indian currency at the airport when you arrive. The current exchange rate is about Rs. 47/- per US dollar. Once in India, you can buy additional Indian currency from local branches of Citibank, Thomas Cook, etc. However, it is typically difficult to convert Indian currency back into foreign currency because of exchange regulations.

Hotel Reservations:
Please make your hotel reservations ahead of time so as to get your choice of accommodation. Check the conference website for information about accommodations. You may also find attractive rates on the web.

Time and Weather
The Indian Standard Time (IST) is 5 1/2 hours ahead of the Greenwich Mean Time(GMT) and is 13 1/2 hours ahead of the U. S. Pacific Standard Time(PST). In December/January, the weather is mildly tropical with temperatures averaging about 28° Celsius (approx. 82° Fahrenheit) during the day and about 15° Celsius (approx. 59° Fahrenheit) during the night.

Sunrise – 6:10 am (approx.)
Sunset – 5:15 pm (approx.)

For detailed local information, visit the HiPC website at http://www.hipc.org/hipc2001. Check out the local info and accommodation sections.

Airport to Hotel Transportation
The airport is 7 kms (approx. 4 miles) from Taj Krishna and Taj Residency. The taxi fare can vary. One way prepaid taxi fare is approximately Rs. 225 plus tip (Rs. 350 for an air-conditioned car).

High Performance Computing 2001
University of Southern California, EEB 200C
Los Angeles, CA 90089-2562, USA

Co-sponsored by:

Indian Institute of Information Technology, Hyderabad
European Association for Theoretical Computer Science
IEEE Computer Society
Technical Committee on Parallel Processing
ACM SIGARCH

HiPC 2002 will be held December 17-20, 2002 in Bangalore, India.